IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#10 Appeal Brief
T. Young
10-31-00

Applicant: Hanratty et al

Serial No.: 09/092,115

Filed: 06/05/98

Docket: TI-25277

Art Unit: 2823

Examiner: Hawranek

For: Antireflective Structure and Method

APPELLANTS' BRIEF (in triplicate)

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 today.

Gracia Sansom 10-17-00

Gracia Sansom Date

Assistant Commissioner
for Patents
Washington, DC 20231

Dear Sir:

The attached sheets contain the Rule 192(c) items of appellants' brief. The Commissioner is hereby authorized to charge the fee for filing a brief in support of the appeal plus an extension of time (separate petition enclosed) and any other fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668; two additional copies of this first sheet of appellants' brief are enclosed.

Respectfully submitted,

Carlton H. Hoel
Reg. No. 29,934
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972.917.4365

Rule 192(c)(1) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 192(c)(2) Related appeals and interferences

Related copending application serial no. 08/678,847 is on appeal.

Rule 192(c)(3) Status of claims

Claims 1-4 are pending in the application with all claims finally rejected. This appeal involves all finally rejected claims.

Rule 192(c)(4) Status of amendments

There is no amendment after final rejection.

Rule 192(c)(5) Summary of the invention

The invention provides a method of integrated circuit fabrication with transistor gates having a gate length less than the linewidth provided by the lithography in conjunction with interconnects or gate tops with linewidth as provided by the lithography. In particular, Fig. 1d shows photoresist patterned to the provided linewidth; Fig.1e shows reduction of the photoresist linewidth; Fig.1g shows gate (or dummy gate) formed by etching with the reduced photoresist as mask; Fig.1i shows the gate (or dummy gate) with sidewall dielectric; Fig.5a shows the dummy gate with adjacent dielectric; and Fig.5c shows the dummy gate removed and a gate with top portion having linewidth provided by the lithography. Application page 4, paragraph (5) describes photoresist linewidth reduction, and page 9 describes the dummy removal and T-shaped gate formation. This method allows the typically smallest linewidth (the gate length) to be sublithographic in conjunction with standard lithography.

Rule 192(c)(6) Issues

The issues presented on appeal are:

(1) whether claims 1-3 are patentable over the Auda and Wolf references.

(2) whether claim 4 is patentable over the Mishra, Auda, and Maniar references.

(3) whether claim 1 constitutes double patenting over claims 1-5 of copending application serial No. 08/678,847.

Rule 192(c)(7) Grouping of the claims

The claims are treated as single group in each rejection.

Rule 192(c)(8) Argument

(1) Claims 1-3 were rejected as unpatentable over Auda in view of Wolf. The Examiner asserted that Auda shows isotropic photoresist linewidth reduction for etching gates, that Wolf shows photoresist without linewidth reduction for etching interconnects over gates, and that Auda would inherently use Wolf to complete a device.

Appellants reply that Auda would inherently apply the same photoresist linewidth reduction to the interconnect formation as to the gates. Indeed, the point of the photoresist linewidth reduction is to achieve linewidths less than direct photolithography can yield. The references fail to suggest such a use of both reduced and nonreduced linewidths. Thus claim 1 and its dependencies are patentable over the references.

(2) Claim 4 was rejected as unpatentable over Mishra in view of Auda and Maniar. The Examiner cited Fig.2e item 48 of Mishra for photoresist and reducing the width of dummy gates and appied Auda as previously and Maniar for antireflective coatings.

Appellants repeat the argument that the references have no suggestion of the mixed use of photoresist: with and without linewidth reduction. The Examiner is correct that the elements of the claims are notoriously well-known items (interconnect lithography, dummy gate, antireflective coating, and photoresist reduction); but the claims are combinations of such elements. Indeed, the cited Mishra item 48 is not photoresist but a silicon nitride dummy gate which used standard photolithography (column 6, lines 51-54), then is reduced in size (column 6, lines 54-58), and eventually

replaced by a T-shaped gate. Thus Mishra suggests the opposite of the claimed linewidth reduction of the photoresist prior to dummy gate formation and is inconsistent with Auda who also reduces the photoresist prior to gate formation. The references disclose the elements but fail to suggest the claimed combinations.

(3) Claim 1 was provisionally rejected under the judicial doctrine of double patenting with respect to claims 1-5 of copending application serial no. 08/678,847. Appellants will submit any necessary terminal disclaimer when claims of the copending application are allowed; note copending application 08/678,847 is on appeal. However, the claims of the copending application relate only to steps (a)-(c) of independent claims 1 and 4 of the present application; and thus the provisional double patenting rejection essentially repeats the rejections based on the references.

Rule 192(c)(9) Appendix

1. A method of fabricationof an intergrated circuit, comprising the steps of:

(a) patterning a first layer of resist on a layer of gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form gates from said layer of gate material;

(d) forming a layer of dielectric on said gates;

(e) patterning a second layer of photoresist to define interconnects;

(f) using said patterned photoresist without linewidth reduction to form interconnects over said gates.

2. The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask for an underlying layer of metal.

3. The method of claim 1, wherein:

(a) said using of step (f) of claim 1 is using the patterned photoresist as an etch mask to etch grooves in underlying dielectric to be filled with metal.

4. A method of fabricationof an intergrated circuit gate, comprising the steps of:

(a) patterning a first layer of resist on an antireflective layer on a layer of dummy gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form dummy gates from said layer of dummy gate material;

(d) forming a layer of dielectric adjacent said dummy gates;

(e) removing said dummy gates;

(f) depositing gate material on said dielectric and

(g) patterning a second layer of photoresist on a second antireflective layer on said gate material to define gates;

(f) using said patterned photoresist without linewidth reduction to form gates.